REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1, 3, 5-7 and 9-25 are pending. Claims 1, 3, 5-7 and 9-25 stand rejected.

Claims 1, 10, 11, 15, 18, 19, 24, and 25 have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

35 U.S.C. § 112 Rejections

Claims 1, 3, 5-7, 9-25 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 1, 3, 5-7, 9-25 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants have amended specification in a manner set forth above to overcome the Examiner's rejections under 35 U.S.C. § 112, first paragraph. Applicants respectfully request the Examine to withdraw the rejection.

Claims 1, 3, 5-7, 9-25 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants have amended specification in a manner set forth above to overcome the Examiner's rejections under 35 U.S.C. § 112, second paragraph. Applicants respectfully request the Examine to withdraw the rejection.

35 U.S.C. § 103 Rejections

Claims 1, 3, 5, 9-13, 19-25 and 8-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No.: 6,535,798 B1 of Bhatia, et al. ("Bhatia"), or US Patent No. 5,835,885 of Lin ("Lin") in view of Hafizi of "Reliability of ALInAs / GaInAs heterojunction bipolar transistors" or U.S. Patent No. 5,798,667 of Herbert ("Herbert") or US Patent No. 6,393,374 of Rankin, et al., ("Rankin"). Claims 6-7, 14-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bhatia or Lin in view of Hafizi or Herbert or Rankin and further in view of US Patent No. 6,373,768 B2 of Woo, et al., ("Woo") or US Patent No. 5,953,685 of Bogin, et al. ("Bogin").

Applicants have amended claim 1 to particularly point out that a maximum allowable data transfer rate is calculated based on the sustainable power level. The operation of the integrated circuit is adjusted such that the maximum allowable data transfer rate is not exceeded.

Bhatia discloses switching an operation of a processor between a high frequency (high performance state) and a low frequency (low performance state) when an over temperature condition is detected by a temperature monitoring device. More specifically, Bhatia discloses

> In the HP state, a processor's (or other component's) core clock frequency and voltage level may be at one setting, while in the LP state, the processor's core clock frequency and voltage level may be at a lower setting. The thermal management scheme is designed to increase the amount of time the processor (or other component) is operating in the HP state. The processor (or other component) spends a programmed percentage of time in the LP state (throttled or non-throttled) and the rest of the time in the HP state. This is

referred to as cycling between the HP and LP states when an over-temperature condition exists.

(Bhatia, col. 2, lines 45-55) (emphasis added)

Further, Bhatia discloses

> One or more temperature sensor units 15 monitor system temperature in one or more corresponding thermal zones, each capable of issuing an interrupt, e.g., a system management interrupt (SMI), a system controller interrupt (SCI), or some other notification when a sensed temperature rises above a preset target temperature Tt or falls below the target temperature Tt. Furthermore, to effect the thermal management scheme according to an embodiment of the invention, periodic interrupts are generated to indicate if the sensed temperature remains below or above the target temperature Tt. Alternatively, a device driver or other software or firmware layer or module may be used to monitor the monitored temperature and to generate thermal management interrupts when appropriate.

(Bhatia, col. 3, lines 33-46) (emphasis added)

Thus, Bhatia merely discloses switching a frequency of the processor from a high frequency setting to a low frequency setting in response to interrupts issued by temperature sensors, in contrast to calculating a maximum allowable data transfer rate based on the sustainable power level of the processor, as recited in amended claim 1. As such, Bhatia fails to disclose, teach, or suggest calculating a maximum allowable data transfer rate based on the sustainable power level. Additionally, Bhatia fails to disclose, teach, or suggest adjusting operation of the integrated circuit such that the maximum allowable data transfer rate is not exceeded.

Lin discloses slowing down the speed of the CPU when an over temperature condition is detected by a heat sensitive resistance. More specifically, Lin discloses

> As the working temperature of CPU 30 rises, the value of temperature sensing heat sensitive resistance 70 decreases linearly, and the potential of a resistor connected to its one terminal will inverse proportionally increase to a starting value as soon as the working temperature of CPU 30 reaches a predetermined value. Then an over temperature actuating circuit 80 is actuated and outputs a signal (LO) to an over temperature alarm circuit 90 for energizing it. At this time since both the pre-located

functional ON/OFF circuit 50 and the over temperature alarm circuit 90 are cascadely grounded, an audio frequency alarm circuit 100 is energized and outputs a sound alarm, and the signal (LO) is sent to a chip circuit 40 via another circuit for the chip circuit 40 to output a (REFRESH) signal to a frequency eliminating circuit 110 to initiate it. At this time the output from the frequency eliminating circuit 110 is input to a frequency eliminating control circuit 120 to split the (SYSCLK) signal which is coming from the front of chip circuit 40, and control the (STPCLK) terminal 31 of CPU 30 with said split (SYSCLK) signal to slow down the operation speed of CPU 30. The heat generated from CPU 30 is therefore reduced to the extent which is able to assure CPU 30 to work continuously and keep effectively the information on line.

(Lin, col. 2, lines 38-61) (emphasis added)

Thus, Lin merely discloses slowing down a speed of the CPU in response to overheating condition detected by a temperature sensitive resistor, in contrast to calculating a maximum allowable data transfer rate based on the sustainable power level of the CPU, as recited in amended claim 1. As such, Lin fails to disclose, teach, or suggest calculating a maximum allowable data transfer rate based on the sustainable power level. Additionally, Lin fails to disclose, teach, or suggest adjusting operation of the integrated circuit such that the maximum allowable data transfer rate is not exceeded, as recited in amended claim 1.

Hafizi merely discloses experimentally determining a junction temperature of AlInAs/GaInAs heterojunction bipolar transistors (Hafizi, Abstract), and similarly to Bhatia and Lin, fails to disclose, teach, or suggest discussed above limitations of amended claim 1.

Herbert merely discloses using the output of the temperature comparator circuit to change an operating frequency for a CPU if a measured temperature of the CPU exceeds a threshold value (col. 4, lines 52-65), in contrast to calculating a maximum allowable data transfer rate based on the sustainable power level, as recited in amended claim 1. Additionally, Herbert fails to disclose, teach, or suggest adjusting operation of the integrated circuit such that the maximum allowable data transfer rate is not exceeded, as recited in amended claim 1.

Rankin merely discloses switching a clock signal to an integrated circuit off if a temperature measured by a temperature sensor exceeds a predetermined value (Figure 4, col. 5 lines 45-50), and similarly to Bhatia, Lin, Hafizi, and Herbert fails to disclose, teach, or suggest discussed above limitations of amended claim 1.

Woo merely determining the operating temperature of the device, and changing the operation mode of the memory device based on the determined temperature (see e.g., Abstract, col. 5, lines 10-24, col. 8 lines 27-42), in contrast to calculating a maximum allowable data transfer rate based on the sustainable power level of the device, as recited in amended claim 1. Additionally, Woo fails to disclose, teach, or suggest adjusting operation of the integrated circuit such that the maximum allowable data transfer rate is not exceeded, as recited in amended claim 1.

Bogin merely discloses monitoring the access rate of data transfer requests to system memory, and limiting the data transfer requests when the access rate is greater than a predetermined threshold, and similarly to Bhatia, Lin, Hafizi, Herbert, Rankin, Woo, and Bodin, fails to disclose, teach, or suggest discussed above limitations of amended claim 1.

Thus, neither Bhatia, Lin, Hafizi, Herbert, Rankin, Woo, or Bodin discloses, teaches, or suggests limitations of amended claim 1 of calculating a maximum allowable data transfer rate based on the sustainable power level of the device, as recited in amended claim 1. Additionally, neither Bhatia, Lin, Hafizi, Herbert, Rankin, Woo, or Bodin discloses, teaches, or suggests limitations of amended claim 1 of adjusting operation of the integrated circuit such that the maximum allowable data transfer rate is not exceeded.

Consequently, even if the references cited by the Examiner were combined, such a combination would lack such limitations of amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over Bhatia or Lin, in view of Hafizi or Herbert or Rankin, and in further view of Woo or Bogin.

Because amended independent claims 11, 15, 19, 24, and 25 contain at least the discussed above limitations of amended claim1, Applicants respectfully submit that claims 11, 15, 19, 24, and 25 are likewise not obvious under 35 U.S.C. § 103 (a) over Bhatia or Lin, in view of Hafizi or Herbert or Rankin, and in further view of Woo or Bogin.

Given that claims 3, 5-7, 9-10, 12-14, 16-18, and 20-23 depend, directly or indirectly, from respective amended claims 1, 11, 15, and 19, and add additional limitations, Applicants respectfully submit that claims 3, 5-7, 9-10, 12-14, 16-18, and 20-23 are likewise not obvious under 35 U.S.C. § 103 (a) over Bhatia or Lin, in view of Hafizi or Herbert or Rankin, and in further view of Woo or Bogin.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 11/7/05 By: _____

Michael J. Mallie
Reg. No.: 36,591

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8300